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REMARKS/ARGUMENTS

In the Detailed Action, all of the rejections of claims 1-25 rely on Collmeyer et al. U.S. Patent No. 7,024,649. The present invention as claimed is directed to a graphical interface method. The Detailed Action contends that Collmeyer et al. teaches a graphical interface, but this contention is completely wrong and is not supported by the disclosure of Collmeyer et al. There is no disclosure or teaching anywhere in Collmeyer et al. of any graphical interface as recited in the claims of this application.

Consequently, all of the claim rejections are unsupported by the disclosure of Collmeyer et al. and appear to be based on an incorrect understanding of this reference. Accordingly, the rejections are unjustified and improper.

The claim rejections with respect to individual claims are addressed below in the same sequence as in the Detailed Action.

Claims 1-5, 12, 14-22, and 25 rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Collmeyer et al.

Claim 1

Claim 1 is directed to "A graphical interface method ...". The Detailed Action contends that:

"Collmeyer et al. teaches:

A graphical interface (host interface - see e.g., col. 3, lines 13 - 18 and col. 12, line 51; i.e., the host interface generates the schematic of the desired power supply) method ..."

This contention is not correct. Collmeyer et al. does not disclose or suggest anywhere any graphical interface.

Collmeyer et al. actually states at col. 3, lines 13 - 18:
"After a particular alternative is selected, the tool creates the schematic of the desired power supply and generates the data necessary to manufacture, configure, or operate the control subsystem including the control component or components of the supply."

There is no reference here to any display or graphical interface. It is clear from this that the design "tool creates the schematic". The nature of this is clarified by subsequent passages at col. 3, lines 19-41 reciting (underlining added):

"The tool generates control subsystem designs for any of three target implementations, where each target implementation implies a different realization strategy for the control subsystem. In a first target implementation, a portion of the control subsystem is provided in a net list form suitable for the realization of an application specific integrated circuit (ASIC). Instructions for the manufacture of such application specific controller components may be generated.

"In a second target implementation, a portion of the control subsystem is provided as information to configure an off-the-shelf, user-configurable controller. The tool searches a library of off-the-shelf controller information to select the optimal controller or combination of controllers. Configuration information is generated that configures the selected controller or controllers to operate in conformance with the designer's specifications.

"In a third target implementation, a portion of the control subsystem is provided in a net list form suitable for the customization of one or more programmable logic devices in a rapid prototyping system constructed for prototyping multi-input, multi-output power supplies."

It is clear from these passages that Collmeyer et al.'s design tool as disclosed in col. 3 produces information, for example in the form of a net list, for the selection, configuration, and manufacture for realizing a desired control subsystem. There is no disclosure or suggestion here of any graphical interface. The "host interface" referred to in the Action in this respect is also not referred to in these passages.

Col. 12, line 51 of Collmeyer et al. referred to in the Action states:
"A host interface (described below) is used to alter the value of the register and thus control the feature."

Again, there is no disclosure here of any graphical interface as claimed. The nature of the "host interface" refereed to in Collmeyer et al. is described at col. 18, lines 11-28 under the heading "Host Communications Link", which makes it clear that the "host interface" is a communications interface. Specifically, this passage recites:

"Host Communications Link
"A host interface may optionally be incorporated into the design, as in FIG. 8 item 200. The host interface allows an external agent, such as a microprocessor, to interrogate the status and control various aspects of a generated power supply. An optional parameter input to the design tool controls the presence or absence of a host interface, and other optional parameters can control the details of the functioning of the interface itself. Possible interface options include well-known industry standard communications links such as Universal Serial Bus (USB) and Inter-integrated circuit (I.sup.2C), RS-232, and others. Other possible options might be on-chip interfaces including one or more of the proposed standard on-chip interconnection buses such as the Virtual Component Interface from the Virtual Socket Interface Alliance (VSIA) and others. Lastly, a non-industry standard interface comprising a minimum of connecting logic may be provided."

Thus it is clear that in Collmeyer et al. the "host interface" is a communications interface to an external agent such as a microprocessor. Again, there is no disclosure or suggestion of any graphical interface as claimed in the present application.

The contention in the Action that "the host interface generates the schematic of the desired power supply" is not correct, and even if it were correct does not disclose or suggest a graphical interface as claimed.

Claim 1 specifically recites "displaying on a display device a graphical display representing the topology of the power system". This is also not disclosed or suggested by Collmeyer et al.

In this respect the Action refers to Collmeyer et al. allegedly disclosing "displaying on a display device (display - see e.g. col. 23, line 45) a graphical display representing the topology of the power system (see e.g. Fig. 3 and col. 5, lines 41 - 57);".

Collmeyer et al. actually states at col. 23, lines 44-47 that "The electrical power supply system can be monitored by a console that comprises a display for indicating the different voltages generated by the configurable power sources." There is again no disclosure or suggestion here of any graphical display, and certainly not of any graphical display representing the topology of the power system. The described display is only "for indicating the different voltages". The paragraph at col. 5, lines 41-57 contains no disclosure of any display, and specifically not a graphical display representing the topology of the power system as recited in claim 1.

Fig. 3 of Collmeyer et al., referred to in the Action, illustrates a power supply topology, but there is no disclosure or suggestion in Collmeyer et al. of displaying such a topology on a graphical interface, as required by the wording of claim 1.

Claim 1 further recites "displaying on the display device a graphical display representing the sequencing of the plurality of power supplies". This is also not disclosed or suggested by Collmeyer et al.

In this respect the Action refers to Collmeyer et al. allegedly disclosing "displaying on the display device (display - see e.g. col. 23, line 45) a graphical display representing the sequencing of the plurality of power supplies (see e.g., see e.g., Fig. 3 and col. 21, lines 1 - 16; i.e. the graphical display of the sequencing and plurality of power supplies are displayed on host interface);".

The same comments as above apply to the display device referred to in col. 23: there is no disclosure of a graphical display, and specifically not of "a graphical display representing the sequencing of the plurality of power supplies" as recited in claim 1. Fig. 3 of Collmeyer et al. does not disclose sequencing or any display of sequencing of power supplies. Col. 1, lines 1-16 of Collmeyer et al. discuss sequencing, but do not disclose or suggest "a graphical display representing the sequencing of the plurality of power supplies" as recited in claim 1.

Thus claim 1 clearly recites numerous features of the invention claimed therein that are not disclosed or suggested by Collmeyer et al. The same applies to each of the dependent claims 2 to 16 in view of the dependency of these claims from claim 1.

Claim 4

This claim adds a recital of "displaying icons representing the plurality of power supplies and paths extending to and from the icons representing input and output voltage lines of the power supplies". These steps are not disclosed or suggested by Collmeyer et al.

In this respect the Action refers extensively to Fig. 3 of Collmeyer et al., along with col. 3, lines 50-61; col. 4, lines 9-11; connection 315 and col. 20, line 67; and Vout1 to Vout5 in Fig. 3. However, none of these disclose or suggest any graphical display, or displaying icons and paths as recited in claim 4.

There appears to be some misunderstanding by the Examiner with respect to the illustration in Fig. 3 of Collmeyer et al. As stated in Collmeyer et al. at col. 4, lines 9-11: "FIG. 3 is a block diagram illustrating a multi-output power supply control subsystem incorporating a multi-output controller or multi-controller". This is not a disclosure or suggestion of displaying such a block diagram in the design tool disclosed and taught by Collmeyer et al. There is no disclosure or suggestion of such a display in Collmeyer et al., nor is there any disclosure of any graphical interface or display device for such displaying.

By the comments in the Action, the Examiner appears to be contending that Collmeyer et al., by illustrating certain things in Fig. 3, is disclosing that these things are displayed by the design tool. This is clearly not the case.

Claim 5

Similar comments apply with respect to claim 5 in view of its dependency upon claim 4, and in view of its own recitals. Again, Fig. 3 of Collmeyer et al. is a block diagram illustrating a power supply arrangement, it is not a disclosure that such a diagram is displayed by the tool described in Collmeyer et al.

Claim 15

Similar comments also apply with respect to claim 15 reciting that "the steps of displaying comprise representing different types of power supply by different icons". Here it is observed that in Fig. 3 of Collmeyer et al. all of the power stages are represented by the same size and shape of rectangle, not "in different length and height" as contended in the Action, but in any event there is no disclosure or suggestion in Collmeyer et al. of any display of information as shown in that Fig. 3.

Claim 18

This claim, like claim 1 as discussed above, is directed to "A graphical interface method" which is not disclosed or suggested by Collmeyer et al. as discussed above in relation to claim 1. Further, claim 18 specifically recites:

"displaying on a display device a graphical display representing the topology and sequencing of the plurality of power supplies of the power system".

As discussed above in relation to claim 1, Collmeyer et al. does not disclose or suggest any display device for a graphic display, and does not disclose any step of displaying a graphical display representing the topology and sequencing of the plurality of power supplies of the power system.

In this respect the Action refers to the same parts of Collmeyer et al. as already discussed above in relation to claim 1, and the same comments as above apply.

Claim 19

This claim likewise is directed to "A graphical interface method" and specifically recites "displaying on a display device a graphical display representing the power supplies and their sequencing". Again, as discussed above in relation to claims 1 and 18 there is no disclosure or suggestion in Collmeyer et al. of either a graphical interface or such a step of displaying a graphical display.

In this respect the Action refers for example to col. 6, lines 39-48 of Collmeyer et al. which includes the statement: "The designer views the design information and may alter the power supply parameters 2, thus causing the tool to select a new design." Other passages in Collmeyer et al. refer to the designer viewing simulation output. There is no disclosure or suggestion in Collmeyer et al. of any graphical interface or graphical display of information. On the contrary, this passage at col. 6 states: "The preferred design is in the form of a digital/analog design file 7, from which the user can extract comprehensive design information, including system level schematics, performance specifications, bills of material, and control subsystem on-chip design output.". "A digital/analog design file" as recited in Collmeyer et al. is not a graphical display of information as recited in claim 19.

Claims 20 to 22

Substantially the same comments as made above in relation to claims 4, 5, and 15 also apply to these claims, as well as the above comments in relation to claim 19 from which these claims depend.

Claims 6-11, 23, and 24 rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Collmeyer et al. in view of Boros et al. US Patent No. 7,135,789, and claim 13 rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Collmeyer et al. in view of Lee et al. Publication No. 2005/0010872

Claims 6-11, 13, 23, and 24 are all dependent claims to which the same comments apply as made above in relation to the respective claims from these claims depend. Boros et al. and Lee et al. do not add to the disclosure of Collmeyer et al. anything of particular relevance in these respects.

For at least the above reasons, it is respectfully submitted that all of claims 1-25 of this application are properly allowable, and the Applicant therefore respectfully requests that a timely Notice of Allowance be issued in this application.

In view of the foregoing, early favorable consideration of this application is earnestly solicited.

Respectfully submitted,

AVINASH CHIDAMBARAM, ET AL

By _____

Elliott S. Simcoe
Reg. No. 50,010
Tel.: (613) 232-2486

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RJH/ESS/wfs